



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,859	11/29/2001	Bruce Allan Makinen	10011248-1	6699

7590 08/23/2005  
AGILENT TECHNOLOGIES, INC.  
Legal Department, DL429  
Intellectual Property Administration  
P.O. Box 7599  
Loveland, CO 80537-0599

EXAMINER

AMINI, JAVID A

ART UNIT	PAPER NUMBER
----------	--------------

2672

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/997,859

Applicant(s)

MAKINEN, BRUCE ALLAN

Examiner

Javid A. Amini

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-13 and 19-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Response to Arguments***

Applicant's arguments filed 3/14/05 have been fully considered but they are not persuasive accept the double patenting issue, which has been withdrawn.

Applicant on page 11 re. independent claim 6 argues the reference Weisgerber does not teach “displaying a target area containing the first image object selected, the target area corresponding to a portion of the printed circuit board to be imaged by an x-ray imaging system”

Examiner's reply: Weisgerber in paragraphs 0058-0059 teaches an AOI i.e. Area of Interest, (Any inspection box or feature). Blob Image: A two-dimensional pixel array used as a mask for 2-D and 3-D image data. Pixels that touch or are related are coded with like values. Generally formed via thresholding techniques and application of a connected component algorithm.

Applicant on the same page argues the reference does not tech the feature of a “target area” at all.

Examiner's reply: Weisgerber in paragraphs 0058 teaches an AOI i.e. Area of Interest, (Any inspection box or feature). The paragraph is actually disclosed an AOI i.e. equivalent to a target area.

Applicant at first paragraph on page 12 argues the reference does not disclose “modifying the displayed target area such that the target area is automatically manipulated to contain the first and second image objects”.

Examiner's reply: Interpretation: Applicant claims the target area i.e. second image, and the first image i.e. the whole image, are displayed the same time. The reference discloses the AOI *id*, the AOI is a portion of a larger image i.e. equivalent to the first image that Applicant claims.

Therefore the claims' features are obvious. The reference teaches at paragraph 0011 X-ray

Art Unit: 2672

inspection can be used at the end of the line to find solder joint and placement defects. However, this is at the last stages of the SMT process and thus the least cost effective. The SMT or hybrid circuit is an electronic circuit composed of different types of integrated circuits and discrete components, mounted on a ceramic base. Used in military and communications applications, it is especially suited for building custom analog circuits including A/D and D/A converters, amplifiers and modulators. They are fixable through automated process.

Applicant on pages 12-15 argues similar matter as previously mentioned.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-13 and 19-42 rejected under 35 U.S.C. 103(a) as being unpatentable over Weisgerber et al. (hereinafter refers as Weisgerber), and further in view of Primrose.

1. Claim 6 also claims 19, 27 and 28 are similar to the limitations of claim 6,

Weisgerber in paragraph 0018-0021 teaches the step of: A method for manipulating a graphical display of a printed circuit board model, the printed circuit board model adapted to be used in an automated x-ray inspection system for detecting defects in a manufactured printed circuit board having one or more components comprising one or more pins soldered to the printed circuit board, the method comprising the steps of: Weisgerber in paragraph 0024 teaches the step of providing a graphical user interface comprising a first portion for providing a graphical

Art Unit: 2672

display of a printed circuit board model comprising a plurality of image objects associated with a printed circuit board; Weisgerber in fig. 1 at block 24 illustrates receiving a user selection of a first image object in the first portion of the graphical user interface; and Weisgerber in fig. 2 at block 26 illustrates 3-D data is acquired in an area of interest (AOI) that is similarly equivalent to following claim's features: displaying a target area containing the first image object selected, the target area corresponding to a portion of the printed circuit board to be imaged by the X-ray imaging system; receiving a user selection of a second image object in the first portion of the graphical user interface; and modifying the displayed target area such that the target area is automatically manipulated to contain the first and second image objects. Weisgerber at paragraph 0011 discloses that X-ray inspection can be used at the end of the line to find solder joint and placement defects. However, this is at the last stages of the SMT process and thus the least cost effective. Applicant in fig. 9 illustrates an expensive way of inspection, because the X-ray inspection is used for every circuit board.

However Primrose at paragraph 0010 teaches a ball grid array (BGA) i.e. a ball grid array is a type of surface-mount packaging used for integrated circuits. It is descended from the pin grid array (PGA), which is a package with one face covered (or partly covered) with pins in a grid pattern. These pins are used to conduct electrical signals from the integrated circuit to the printed circuit board (PCB) it is placed on. Primrose in fig. 8 block 802 illustrates performing an inspection of the X-ray to verify connection for every electronic component.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Primrose into Weisgerber in order to incorporate the type of

Art Unit: 2672

surface-mount packaging used for integrated circuits, and performing an inspection of the X-ray to verify connection for every electronic component.

Examiner's suggestion: The following interpretation applies to the last two lines of claim 6: the target area contains the first and second image objects. The terms e.g. "modifying", "automatically", and "manipulated" need to pin point the proper subjects.

2. Claim 7 also claims 20 and 29 which are similar to the limitations of claim 7, Weisgerber in fig. 2 at block 26 illustrates 3-D data is acquired in an area of interest (AOI) that is similarly equivalent to the features in the claims.
3. Claim 8 also claims 21 and 30 which are similar to the limitations of claim 8, The method of claim 6, Weisgerber in fig. 2 at block 26 illustrates 3-D data is acquired in an area of interest (AOI) that is similarly equivalent
4. Claim 9 also claims 22 and 31 which are similar to the limitations of claim 9, Weisgerber in figs. 7c, 8 and 9a illustrates the limitations of claim 6, wherein at least one of the plurality of image objects comprises a family object that specifies a type of solder joint.
5. Claim 10 also claims 23 and 31 which are similar to the limitations of claim 10, Weisgerber in fig. 6b illustrates at least one of the plurality of image objects comprises a package object that specifies a type of component.
6. Claim 11 also claims 24, 32 and 33 which are similar to the limitations of claim 11, Weisgerber in paragraph 0019 teaches the limitations of a unique pin number for a specific component in the printed circuit board. And also it is obvious that each electronic component has a unique pin number.
7. Claim 12 also claims 25 and 34 which are similar to the limitations of claim 12,

Art Unit: 2672

Weisgerber in fig. 4a number 50 illustrates a shape similar to a square.

8. Claim 13 also claims 26 and 35 which are similar to the limitations of claim 13,

Weisgerber in fig. 1 block 22 illustrates high-speed image processing hardware and software processes both 3-D and 2-D data. Therefore, the step of the claims is obvious.

9. Claim 36

The step of centering the target area or as Weisgerber discloses an AOI with respect to the first and second image objects is obvious.

10. Claim 37.

The step is very obvious the way Examiner understood the claim languages. Otherwise Applicant needs to provide more definition about the relationship between the target area and the second image.

11. Claim 38.

The step is obvious. Weisgerber in figs. 7b-c illustrates the claim language.

12. Claim 39.

Weisgerber in the abstract discloses inspecting electronic components mounted on printed circuit boards.

13. Claim 40.

Primrose in fig. 5 illustrates an exemplary BGA connection x-ray with an x-ray visible orientation indicator 500 included in the solder pad 102A. In this work, the orientation indicator 500 is a distinctly shaped contact pad 500 at the "pin 1" connection 102A.

14. Claim 41.

Weisgerber in fig. 4a number 50 illustrates a shape similar to a square

Art Unit: 2672

15. Claim 42.

Weisgerber in fig. 1 block 22 illustrates high-speed image processing hardware and software processes both 3-D and 2-D data. Therefore, the step of the claims is obvious.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A. Amini whose telephone number is 571-272-7654. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



Art Unit: 2672

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



JEFFERY BRIER  
PRIMARY EXAMINER

Javid A Amini  
Examiner  
Art Unit 2672

Javid Amini